FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
1875.2810001/RES/GSB	*To Be Assigned*
FIRST NAMED INVENTOR	
Jan MULDER	
FILING DATE	**ART UNIT**
Herewith	*To Be Assigned*

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
JGW	AA1	6,583,747 B1	06/2003	van der Goes *et al.*	341	156	
	AB1	6,628,224 B1	09/2003	Mulder *et al.*	341	156	
	AC1	6,518,898 B1	02/2003	Choksi	341	118	
	AD1	6,346,902 B1	02/2002	Venes *et al.*	341	154	
	AE1	6,489,913	12/2002	Hansen *et al.*	341	156	
	AF1	6,169,502	01/2001	Johnson *et al.*	341	120	
	AG1	6,259,745 B1	07/2001	Chan	375	285	
	AH1	5,867,116	02/1999	Nakamura *et al.*	341	159	
	AI1	5,973,632	10/1999	Tai	341	156	
	AJ1	5,554,943	09/1996	Moreland	327	065	
	AK1	5,422,642	06/1995	Chung *et al.*	341	118	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL1						Yes No
	AM1						Y s No
	AN1						Y s No
	AO1						Y s No
	AP1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

JGW	AR	1	Miyazaki, *et al.*, "A 16 mW 30Msample/s 10b Pipelined A/D Converter Using a Pseudo-Differential Architecture," *IEEE International Solid-State Circuits Conference 2002*, IEEE, February 5, 2002, 3 pages.
	AS	1	Sushihara *et al.*, "A 7b 450Msample/s 50mW CMOS ADC in 0.3 mm^2," *IEEE International Solid-State Circuits Conference 2002*, IEEE, February 5, 2002, 3 pages.
	AT	1	Dingwall *et al.*, "An 8-MHz CMOS Subranging 8-Bit A/D Converter," *IEEE Journal of Solid-State Circuits*, Vol. SC-20, No. 6, December 1985, pages 1138-1143.

EXAMINER Patricia Wang DATE CONSIDERED 05/01/2004

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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U.S. PATENT DOCUMENTS

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	AA2	5,471,210	11/1995	Wingender *et al.*	341	156	
	AB2	5,302,869	04/1994	Hosotani *et al.*	327	075	
	AC2	5,191,336	03/1993	Stephenson	341	111	
	AD2	5,118,971	06/1992	Schenck	326	032	
	AE2	5,157,397	10/1992	Vernon	341	159	
	AF2	5,006,727	04/1991	Ragosch *et al.*	327	306	
	AG2	4,959,563	09/1990	Schenck	326	027	
	AH2	3,846,712	11/1974	Kiko	330	261	
	AI2	3,697,978	10/1972	Prill	341	12	
	AJ2						
	AK2						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL2						Yes No
	AM2						Yes No
	AN2						Y s No
	AO2						Yes No
	AP2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

AR	2	Abo, A.M. and Gray, P.R., "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," *IEEE Journal of Solid-State Circuits*, Vol. 34, No. 5, May 1999, pages 599-606.
AS	2	Brandt, B.P. and Lutsky, J., "A 75-mW, 10-b, 20-MSPS CMOS Subranging ADC with 9.5 Effective Bits at Nyquist," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 34, No. 12, December 1999, pages 1788-1795.
AT	2	Bult, K. and Buchwald, A., "An Embedded 240-mW 10-b 50-MS/s CMOS ADC in 1-mm^2," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 32, No. 12, December 1997, pages 1887-1895.

EXAMINER [signature] DATE CONSIDERED 05/07/04

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA3						
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	AK3						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL3						Yes No
	AM3						Yes No
	AN3						Y s No
	AO3						Yes No
	AP3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	3	Cho, T.B. and Gray, P.R., "A 10b, 20 Msample/s, 35 mW Pipeline A/D Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 30, No. 3, March 1995, pages 166-172.
	AS	3	Choe, M.-J. *et al.*, "A 13-b 40-Msample/s CMOS Pipelined Folding ADC with Background Offset Trimming," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 35, No. 12, December 2000, pages 1781-1790.
	AT	3	Choi, M. and Abidi, A., "A 6-b 1.3-Gsample/s A/D Converter in 0.35-µm CMOS," *IEEE Journal of Solid-State Circuits*," IEEE, Vol. 36, No. 12, December 2001, pages 1847-1858.

EXAMINER	DATE CONSIDERED
Patrick Wamsley	8/07/04

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA4						
	AB4						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL4						Yes No
	AM4						Yes No
	AN4						Yes No
	AO4						Yes No
	AP4						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

PLW	AR	4	Flynn, M. and Sheahan, B., "A 400-Msample/s, 6-b CMOS Folding and Interpolating ADC," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 33, No. 12, December 1998, pages 1932-1938.
	AS	4	Geelen, G., "A 6b 1.1Gsample/s CMOS A/D Converter," *IEEE International Solid-State Circuits Conference*, IEEE, February 6, 2001, pages 128-129 and 438.
	AT	4	Hoogzaad, G. and Roovers, R., "A 65-mW, 10-bit, 40-Msample/s BiCMOS Nyquist ADC in 0.8 mm^2," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 34, No. 12, December 1999, pages 1796-1802.

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	05/07/04

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA5						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL5						Y s No
	AM5						Y s No
	AN5						Y s No
	AO5						Yes No
	AP5						Y s No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	5	Hosotani, S. *et al.*, "An 8-bit 20-MS/s CMOS A/D Converter with 50-mW Power Consumption," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 25, No. 1, February 1990, pages 167-172.
	AS	5	Ingino, J. and Wooley, B., "A Continuously Calibrated 12-b, 10-MS/s, 3.3-V A/D Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 33, No. 12, December 1998, pages 1920-1931.
	AT	5	Ito, M. *et al.*, "A 10 bit 20 MS/s 3 V Supply CMOS A/D Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 29, No. 12, December 1994, pages 1531-1536.

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA6						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL6						Y s No
	AM6						Y s No
	AN6						Y s No
	AO6						Y s No
	AP6						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	6	Kattman, K. and Barrow, J., "A Technique for Reducing Differential Non-Linearity Errors in Flash A/D Converters, " *IEEE International Solid-State Conference*, IEEE, 1991, pages 170-171.
	AS	6	Kusumoto, K. *et al.*, "A 10-b 20-MHz 30-mW Pipelined Interpolating CMOS ADC," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 28, No. 12, December 1993, pages 1200-1206.
	AT	6	Lewis, S. *et al.*, "A 10-b 20-Msample/s Analog-to-Digital Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 27, No. 3, March 1992, pages 351-358.

EXAMINER	DATE CONSIDERED
Patrick Wamsley	05/09/04

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA7						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL7						Yes No
	AM7						Y s No
	AN7						Y s No
	AO7						Yes No
	AP7						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	7	Mehr, I. And Singer, L., "A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 35, No. 3, March 2000, pages 318-325.
	AS	7	Nagaraj, K. *et al.*, "Efficient 6-Bit A/D Converter Using a 1-Bit Folding Front End," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 34, No. 8, August 1999, pages 1056-1062.
	AT	7	Nagaraj, K. *et al.*, "A Dual-Mode 700-Msamples/s 6-bit 200-Msamples/s 7-bit A/D Converter in a 0.25-µm Digital CMOS Process," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 35, No. 12, December 2000, pages 1760-1768.

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Patrick Wamsley	05/07/04

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA8						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL8						Yes No
	AM8						Yes No
	AN8						Yes No
	AO8						Yes No
	AP8						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	8	Nauta, B. and Venes, A., "A 70-MS/s 110-mW 8-b CMOS Folding and Interpolating A/D Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 30, No. 12, December 1995, pages 1302-1308.
	AS	8	Pan, H. *et al.*, "A 3.3-V 12-b 50-MS/s A/D Converter in 0.6μm CMOS with over 80-dB SFDR," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 35, No. 12, December 2000, pages 1769-1780.
	AT	8	Song, W.-C. *et al.*, "A 10-b 20-Msample/s Low-Power CMOS ADC," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 30, No. 5, May 1995, pages 514-521.

EXAMINER	DATE CONSIDERED
	07/07/04

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA9						
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	AI9						
	AJ9						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL9						Yes No
	AM9						Y s No
	AN9						Yes No
	AO9						Yes No
	AP9						Y s No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	9	Sumanen, L. *et al.*, "A 10-bit 200-MS/s CMOS Parallel Pipeline A/D Converter," *IEEE Journal of Solid-State Circuits,* IEEE, Vol. 36, No. 7, July 2000, pages 1048-1055.
	AS	9	Taft, R. and Tursi, M., "A 100-MS/s 8-b CMOS Subranging ADC with Sustained Parametric Performance from 3.8 V Down to 2.2 V," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 36, No. 3, March 2001, pages 331-338.
	AT	9	van der Ploeg, H. and Remmers, R., "A 3.3-V, 10-b, 25-Msample/s Two-Step ADC in 0.35-µm CMOS," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 34, No. 12, December 1999, pages 1803-1811.

EXAMINER	DATE CONSIDERED
Patrick Wamsley	8/10/04

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	AA10						
	AB10						
	AC10						
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	AI10						
	AJ10						
	AK10						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL10						Y s No
	AM10						Yes No
	AN10						Y s No
	AO10						Y s No
	AP10						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

AR	10	van der Ploeg, H. *et al.*, "A 2.5-V 12-b 54-Msample/s 0.25-μm CMOS ADC in 1-mm^2 With Mixed-Signal Chopping and Calibration," *IEEE Journal of Solid-State Circuits*, Vol. 36, No. 12, December 2001, pages 1859-1867.
AS	10	Vorenkamp, P. and Roovers, R., "A 12-b, 60-Msample/s Cascaded Folding and Interpolating ADC," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 32, No. 12, December 1997, pages 1876-1886.
AT	10	Wang, Y-T. and Razavi, B., "An 8-Bit 150-MHz CMOS A/D Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 35, No. 3, March 2000, pages 308-317.

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA11						
	AB11						
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	AJ11						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL11						Yes No
	AM11						Yes No
	AN11						Yes No
	AO11						Yes No
	AP11						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

AR	11	Yotsuyanagi, M. *et al.*, "A 2 V, 10 b, 20 Msample/s, Mixed-Mode Subranging CMOS A/D Convert r," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 30, No. 12, December 1995, pages 1533-1537.
AS	11	Yu, P. and Lee, H-S., "A 2.5-V, 12-b, 5-Msample/s Pipelined CMOS ADC," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 31, No. 12, December 1996, pages 1854-1861.
AT	11	

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